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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Application Number: 10/765,897

Filing Date: January 29, 2004

Appellant(s): CHEN ET AL.

Rajiv P. Sarathy

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/4/2007 and supplemental appeal brief filed 1/11/2008 appealing from the Office action mailed 6/21/2008.

(1) Real Party in interest

A statement identifying by name the real party interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Pat. 6,754,899	Stoye	06-2004
US Pat. 4,493,036	Boudreau et al	01-1985
US Pat. 6,438,672	Fischer et al	08-2002
US Pub2003/0033490	Gappisch et al	02-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,3-8,10-16,18-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Stoye (US 6754899) in view of Fischer et al (US 6438672) and further in view of Boudreau et al (US 4493036).

As in claim 1, Stoye discloses a data access apparatus comprising: an external memory unit for storing data (Stoye's column 2 lines 25-30, extemal memory, Fig 1: #16), wherein the external memory unit has a second time cycle for performing a task; and a control unit couples with the external memory unit via a memory bus (Stoye's Fig 1:#11 IOP corresponding to the claim's control unit, coupling to Fig 1: #14 memory bus), comprising: a microprocessor unit, having a first time cycle to perform a microprocessor operating (Stoye's Fig 1:#12 PP protocol processor, operating at a first clock cycle, requiring to synchronizing its operations with memory that operating at a second clock cycle, see Stoye's column 1 line 65 to column 2 line 3); and Stoye's column 1 lines 20-25 discloses the microprocessor can issue an access command to access its code and data stored in a memory Fig 1: 15. Obviously, the microprocessor must have a memory interface unit to handle accessing to the memory through the bus (i.e requesting the access, providing addresses for data being access, handling bus protocol etc..). Stoye does not expressly disclose the claim's detail of "an internal memory unit, which is accessible only by the microprocessor unit". However, Fischer discloses a well known hierarchical memory system including an internal memory.unit, which is accessible only by the processor unit (Fischer's Fig 6, column 1 lines 39-52, L1 cache embedded in the processor #604 thus accessed only by processor #604; and larger memory such as L2 and/or main memory #601); Fischer further teaches a memory interface control unit

(Fischer's Fig 6:#602 cache controller) for corresponding transforming an internal data access address of an internal memory unit (Fischer's Fig 6:#603 cache) into a data address of the external memory unit (Fischer's Fig 6:#601 L2/main memory) and thereby the microprocessor unit (Fischer's Fig 6:#604 processor) issuing the internal data access address could access data from the external memory unit via the memory interface control unit (see Fischer's column 1 line 66 to column 2 line 17). It would have been obvious to one of ordinary skill in the art at the time of invention to include the hierarchical memory method and structures as suggested by Fischer in Stoye's system to allow processor to access data quickly in the cache and thereby further improve the overall accessing time for data in the system (see Fischer's column 1 lines 30-39). Stoye further teaches the external memory unit has a data segment storing a flow control parameters and numerical arithmetic of the microprocessor unit (Stoye's column 1 lines 22-23, common memory segment that includes PP code and data, flow table etcc), Stoye further teaches when the microprocessor unit attempts to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit (Stoye's column 1 lines 22-25, PP access the code, data, flow tables) an access request signal issued from the control unit associating with the microprocessor unit against another device for accessing the external memory unit is directed to the external memory unit and the first time cycle is suspended (Stoye's column 1 lines 43-51 discloses a situation in which the PP (corresponding to claim's microprocessor) and IOP (corresponding to the claim's another device) access the shared/common memory; the IOP will be allowed to access the common memory while PP must continue to wait.

Thus Stoye's clearly teaches that during the time IOP accessing data in the common memory, even if the PP requests for access is issued by the PP and forwarding/directing to the common memory, the PP would not be allowed and it must wait/suspended until the IOP complete accessing the common memory, otherwise loss of data may result (see Stoye's column 1 lines 48-51; corresponding to the claim's "an access request signal issued from the control unit .. against another device., is directed (i.e forwarding) to the external memory..").

Stoye and Fischer do not expressly disclose the claim's aspect of an acknowledged signal. However, Boudreau discloses a system of multiple I/O controllers (Boudreau's Fig 1:#103, #104), sharing a main memory (Boudreau's Fig 1:#110) with a processor (Boudreau's Fig 1: # 101), and the associated prioritize circuit to arbitrate memory access requests from these processor, controllers and refresh logic (Boudreau's column 1 lines 36-50). This prioritize circuit provides a signal MEBUSY to the CPU (corresponding to the claim's acknowledge signal) to indicate when CPU may access the data in the memory (i.e when MEBUSY is deasserted). It would have been obvious to one of ordinary skill in the art at the time of invention to include the prioritize circuit and memory busy signal as suggested by Boudreau in Stoye's system modified by Fischer thereby allowing the memory arbitrating the requests in an automatically manner, on the behalf of the CPU, Boudreau's column 12 lines 40-57).

As in claim 3, the claim recites wherein the first time cycle is revived from suspending when the second time cycle is finished. The claim rejected based on the same rationale as of claim 1.

As in claim 4, the claim recites wherein the duration suspending the first time cycle is a time when the external memory unit finishes a current task. The claim rejected based on the same rationale as of claim 1. Boudreau's column 12 lines 40-57 disclose the MEBUSY signal suspends the CPU's memory access until it completes the current memory access.

As in claim 5, Boudreau's column 1 lines 42-50 disclose wherein the external memory unit is dynamic random access memory.

As in claim 6, the claim recites wherein a capacity of the data segment of the external memory unit is smaller that a capacity of the external memory unit. Stoye's column 1 lines 21-25 discloses the external memory contains segments that store PP processor codes, data, data buffers, multiple data structures, multiple flow tables and data structures shared by the IOP and the PP processors. Therefore, the external memory not only contains data segments corresponding to the PP processor, but it also contain data buffers for IOP processor such that IOP processor can use to store data being received from an external peripheral device (see Stoye's column 1 lines 40-43).

As in claim 7, the claim recites wherein data access apparatus could be applied to an optical-electronic system and which is selected from CD-ROM, CD-RW, CD-RW,DVD+/-Rom, DVD+/-RW. Stoye discloses a data access method for a device comprises of an internal processor (Stoye's Fig 1 : PP processor), an IOP processor to receive an external data stream from a peripherals device (Stoye's Fig 1: dev) and storing in a shared memory (Stoye's Fig 1: # 16 main memory has data buffers to receive this external data stream). The main memory further contains data segments

corresponding to the internal processor PP. Stoye teaches that this device can be used as the peripherals device controller to communicate with other peripherals devices. Furthermore, the peripheral device controller by definition includes hard disk drive, tape drive, and optical-magnetic drive such as CD-ROM etc.. Therefore, Stoye clearly suggest this device controller could be applied to an optical-electronic system as claimed.

Claims 8,15 rejected based on the same rationale as of claim 1.

Claims 10,18 rejected based on the same rationale as of claim 3.

Claims 11,19 rejected based on the same rationale as of claim 4.

Claim 12 rejected based on the same rationale as of claim 5.

Claim 13 rejected based on the same rationale as of claim 6.

Claims 14,20 rejected based on the same rationale as of claim 7.

Claim 16 rejected based on the same rationale as of claim 1.

Claims 2,9,17 rejected under 35 U.S.C. 103(a) as being unpatentable over Stoye (US 6754899), Fischer et al (US 6438672), Boudreau et al (US 4493036) as applied to claims 1,8,15 and in view of Gappisch et al (US 2003/0033490).

As in claim 2, the claim recites wherein the first time cycle is much longer than the second time cycle. Stoye, Fishcher and Boudreau do not expressly disclose the memory cycle time "second cycle time" is longer than the processor cycle time "first cycle time". However, it is commonly known in the art that the processors are running at a higher clock frequency than the clock frequency of the memory device. Gappisch's discloses a system comprises multiple processors (Gappisch's Fig 3: CPU_A, CPU_B)

that share a memory device (Gappisch's Fig 3: #Flash memory array), the processors are running at higher clock frequency that that of the memory device (Gappisch's Fig 2: CLK_A, CLK_A and access frequency of memory device TaccFlash). It would have been obvious to one of ordinary skill in the art at the time of invention to include the synchronizing circuit as suggested by Gappisch in Stoye's system modified by Fischer and Boudreau thereby allowing each CPU can synchronizing with the share memory device independently, thereby further increase overall throughput of a system having multiple processing elements, see Gappisch's paragraphs 26 and

Claims 9,17 rejected based on the same rationale as of claim 2.

(10) Response to Argument

Appellant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Appellant's arguments for the following reasons:

A1) With regard to Appellant's arguments for the rejection of claims 1, 3-8, 10-16, and 18-20 under 35 U.S.C. 103 (a), the arguments are not persuasive.

Appellant argues at the appeal brief dated 10/4/2007 pages 13-14,

"With respect to one aspect of the claimed invention, the Examiner alleges that *Fischer* discloses the claimed 'memory interface control unit for correspondingly transforming an internal data access address of an internal memory unit ... into a data address of the external memory unit'. See the last paragraph of page 4

through the first paragraph of page 5 of the Final Office Action. Appellant respectfully submits that *Fischer* does not disclose such claimed limitation, particularly, *Fischer* does not disclose that the memory interface control unit transforms the internal data access address into an external data address as claimed. Specifically, *Fischer* discloses (in FIG. 6 and column 1, line 66 through column 2, line 4) a cache controller 602 (considered by the Examiner to read on the claimed memory interface control unit) which **monitors** the address 605 issued by a processor 604 (considered by the Examiner to read on the claimed microprocessor unit), and then **compares** the address 605 with the address of a cache memory 603 (considered by the Examiner to read on the claimed internal memory unit). Accordingly, what is disclosed in *Fischer* is a cache controller 602 that monitors the address of the processor 604 and compares the monitored address with the address of the cache memory 603. *Fischer* neither indicates nor mentions any '**transforming** an internal data access address of an internal memory unit ... into a data address of the external memory unit' as claimed. A person of ordinary skill in the art would understand that "transform" means to change at least some characteristic of an object. In the claimed invention, the internal address of the internal memory unit is transformed into an external address of the external memory unit (by the memory interface control unit), i.e., not only the address is changed from an internal one to an external one, but the characteristic of the transformed address (for example, the numerical representation of the memory location) is also changed. On the contrary, in

Fischer, the address 605 of the processor 604 is only monitored and then compared with the address of the cache memory 603. No form of address transformation is disclosed or suggested to occur when the *Fischer's* system determines whether the cache hits or misses. Accordingly, a person skilled in the pertinent art would not have been motivated to transform an internal address into an external address based on the disclosure of *Fischer*"

In response, the statement of address transform being "not only the address is changed from an internal one to external one.. but the numeric representation of the memory location is also changed" appears to be redundant. Examiner submits that when an address is changed from [pointing to] an internal memory entity to [point to] an external memory entity, the address value, i.e. the numeric representation of the memory location where the address point to, must be also changed accordingly such that the address value points to the appropriate memory entity. Fischer teaches a hierarchical memory wherein data/object is stored in L1, small fast memory and/or stored in L2, main memory as large slow memory (Fischer's col. 1 lines 39-52. It is noted that the small fast memory can re viewed as claimed internal memory, and the slow large memories can be viewed as claimed external memory). Thus, the numeric representation of the memory location of the data/object in L2/mainmemory must be different with the numeric representation of the memory location of the data/object in L1, simply because they have different memory sizes and thus having different numeric addresses of different address ranges. In other words, if the address value does not

change appropriately in different memories, a wrong location of wrong memory entity would be accessed.

Additionally, Fisher teaches a commonly known in the art of a memory system having an L1 cache 603 corresponds to claim's internal memory entity and an L2 cache 601 corresponds to claim's external memory (col. 1 lines 38-52, "L1 may be a small amount of memory", L2 cache is typically a larger amount of memory external to the processor"), and **further teaches logic for access these memory entities that corresponds to the claim's control unit**, i.e. the cache controller 602 represents the logic for access these memory entities as shown in Fig 6. Fischer teaches that the memory controller logic transform the CPU request of an access to the L1, a fast memory (i.e claimed internal memory unit) **into a separate different request** of an access to the L2/main memory, a slow memory (i.e claimed external memory) when the data object is "cache miss" in L1. In other words, in the event of cache miss, a transformation occurs to transform to a different external request for data/object stored in the L2/main memory, a slow memory (Fig 6, col. 2 lines 10-15, "if the information needed by the processor 604 is not stored in the cache memory 603, a cache miss is said to have occurred and an access to the slower memory 601 must be made, analogous to making another trip to the library").

A2) Furthermore, Examiner notes that the 'transforming" clause can be viewed as an intention of the claimed memory interface control unit. Fischer clearly teaches a memory control logic capable of transforming an internal memory request into an external memory request as discussed above.

Therefore Appellant's argument is not persuasive.

A3) Appellant further argues at the appeal brief dated 10/4/2007 pages 14-15, "With respect to another aspect of the claimed invention, the Examiner alleges in the second paragraph of page 3 of the Final Office Action that *Stoye* discloses (in FIG. 1), the claimed 'control unit' (considered by the Examiner to correspond to IOP 11) and the claimed 'microprocessor unit' (considered by the Examiner to correspond to PP 12). Examiner further alleges in the third paragraph of page 4 of the Final Office Action that *Stoye* further discloses the claimed 'another device' (considered by the Examiner to correspond again to IOP 11), such that 'an access request signal issued from the control unit ... against **another device** accessing the external memory unit' as claimed. Appellant respectfully disagrees with the Examiner's unreasonable reading of the references. Specifically, the **Examiner improperly interprets a single element of *Stoye*, i.e., IOP 11, to read on different claim elements i.e., the claimed 'control unit' and the claimed 'another device' which compete for access to the external memory. A person of ordinary skill in the art would realize that the *Stoye* IOP 11 cannot be considered to compete for memory access against itself, and that the IOP 11 is readable at best only on one, not both, of the claimed 'control unit' and the claimed 'another device.'"** (Emphasis added)

In response, the control unit is described in the claim as having a processing unit and some logic to interface with a memory. Stoye teaches such control unit, i.e IOP 11, because the input-output out processor IOP inherently having a processing unit and

some logic to interface with memory 15 as shown in Fig 1. Thus, the claimed control unit is a device that is taught by Stoye as a processor/device such as IOP or PP because each IOP and PP having a processing unit and some logic to interface with memory 15 ("the IOP and PP are coupled together and to common memory", col. 1 lines 22-24). Because these devices, i.e IOP PP etc.. are coupled to the same common memory, they would compete against among themselves for accessing the same common memory ("col. 1 lines 25-30, "it is therefore possible that conflicts would arise if the two processors both attempted to access the memory at the same time"). In an embodiment, Stoye teaches the competition for a common memory among two processors labeled as IOP and PP. Thus, Stoye teaches the competition of two devices as claimed. In addition, Stoye's col. 5 lines 7-10 further teaches the competition applies equally well with any number of processors sharing access to a common memory, for example a system with several PP's and IOP's and **thus one IOP can compete against another IOP or compete against another PP** etc.. . Again, Stoye clearly teaches the competing of one device against another device for accessing the common memory as claimed ("with more than two processors, some or all may be capable of being assigned higher priority levels if needed", col. 5 lines 7-10).

Therefore Appellant's argument is not persuasive.

The arguments for the rejection of claims 3-8,10-16, and 18-20 are similar to the arguments offered for claim 1 and the same responses apply. As such, these arguments are found to be not persuasive.

B) With regard to Appellant's arguments for the rejection of claims 2,9, and 17 under 35 U.S.C. 103 (a), the arguments are similar to the arguments offered for claim 1 and the same responses apply. As such, these arguments are found to be not persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/ Duc T. Doan/

Duc T. Doan

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